TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	08/520,079
Filing Date	August 28, 1995
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	2815
Examiner Name	Paul E. Brock, II
Total Number of Pages in This Submission: 29	Attorney Docket Number: 740756-1400

ENCLOSURES *(check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Request For Reconsideration
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
  - ☐ Information Disclosure Statement
  - ☐ PTO-1449 w/10 refs.
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Declaration and Power of Attorney
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Communication to Group (Appeal Notice, Brief, Reply Brief)
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Application Data Sheet
- ☐ Request for Corrected Filing Receipt with Enclosures
- ☐ A self-addressed prepaid postcard for acknowledging receipt
- ☐ Other Enclosure(s) (*please identify below*):

Remarks

☒ The Commissioner is hereby authorized to charge any additional fees required or credit any overpayments to Deposit Account No. 19-2380 for the above identified docket number.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm *or* Individual name	**Jeffrey L. Costellia, Reg. No. 35,483** Nixon Peabody LLP 401 9th Street, N.W. Suite 900 Washington, D.C. 20004-2128
Signature	
Date	December 12, 2005

CERTIFICATE OF MAILING OR TRANSMISSION [37 CFR 1.8(a)]

I hereby certify that this correspondence is being:

- ☐ deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop , Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450
- ☐ transmitted by facsimile on the date shown below to the United States Patent and Trademark Office at (703) _____.

_____ Date

_____ Signature

Docket No.: 740756-1400

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Patent Application of	)	Confirmation No.: 1321
Shunpei YAMAZAKI, et al.	)	
Serial No. 08/520,079	)	Examiner: Paul E. Brock II
Filed: August 28, 1995	)	Art Unit: 2815
For: SEMICONDUCTOR CIRCUIT FOR	)	
ELECTRO-OPTICAL DEVICE AND	)	Date: December 12, 2005
METHOD OF MANUFACTURING	)	
THE SAME	)	

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 35 U.S.C. §134 and 37 C.F.R. §41.37, Appellants submit this Appeal Brief in triplicate in support of the Notice of Appeal filed May 17, 2005, to appeal the Examiner's final rejections in the Final Office Action of February 17, 2005, and in response to the Notifications of Non-Compliant Appeal Brief of August 29, 2005 and November 14, 2005.

I. REAL PARTY IN INTEREST

Semiconductor Energy Laboratory Co., Ltd. is the assignee and real party in interest.

II. RELATED APPEALS AND INTERFERENCES

There are presently no appeals or interferences known to the Appellants, the Appellants' representative, or the assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

For the purposes of this Appeal, claims 73-116, 123-141, and 143-155 have been rejected and claims 1-72, 117-122, and 142 have been canceled. Thus, this Appeal is taken from the rejection of claims 73-116, 123-141, and 143-155, as submitted in the Appendix herewith.

IV. STATUS OF AMENDMENTS

No amendments have been made to the claims subsequent to the final rejections stated in the final Office Action of February 17, 2005.

V. SUMMARY OF CLAIMED SUBJECT MATTER

This Appeal is taken from claims 73-116, 123-141, and 143-155, of which claims 73, 80, 87, 93, 99, 105, 111, 123, and 129 are independent.

Independent claim 73 relates to a thin film transistor comprising a crystalline semiconductor island over a substrate (See, for example, reference number 101 in Fig. 3A) having an insulating surface, source and drain regions in said semiconductor island, a channel forming region (See, for example, reference number 109 in Fig. 3C) between said source and drain regions, a gate insulating film (See, for example, reference number 112 in Fig. 3C) adjacent to at least said channel forming region, and a gate electrode (See, for example, reference number 113 in Fig. 3C) in adjacent to said channel forming region having said gate insulating film therebetween, wherein said channel forming region has no grain boundary, wherein said semiconductor island includes a spin density not higher than 1×10^{17} cm^{-3}, and wherein said crystalline semiconductor island includes at least one of hydrogen and halogen element at concentration not higher than 1×10^{20} cm^{-3}. (See, for example, Figs. 2A, 2B, 4B, and 7, and related discussions on page 21, third and fourth paragraphs).

Independent claim 80 relates to a thin film transistor comprising a crystalline semiconductor island on an insulating surface, source and drain regions in said semiconductor island, a channel forming region (See, for example, reference number 109 in Fig. 3C) between said source and drain regions, a gate insulating film (See, for example, reference number 112 in Fig. 3C) on at least said channel forming region, and a gate electrode (See, for example, reference number 113 in Fig. 3C) over said channel forming

region having said gate insulating film therebetween, wherein said channel forming region has no grain boundary, and wherein said semiconductor island includes a point defect of 1 x 10^{16} cm^{-3} or more, and at least one of hydrogen and halogen element at concentration not higher than 1 x 10^{20} cm^{-3}. (See, for example, Figs. 2A, 2B, 4B, and 7, and related discussions on page 21, third and fourth paragraphs).

Independent claim 87 relates to a semiconductor device comprising a crystalline semiconductor island on an insulating surface, source and drain regions in said semiconductor island, a channel forming region (See, for example, reference number 109 in Fig. 3C) between said source and drain regions, a gate insulating film (See, for example, reference number 112 in Fig. 3C) adjacent to at least said channel forming region, and a gate electrode (See, for example, reference number 113 in Fig. 3C) adjacent to said channel forming region having said gate insulating film therebetween, wherein said crystalline semiconductor island is formed in a monodomain region (See, for example, reference number 104 in Fig. 2B) which contains no grain boundary, wherein at least one of hydrogen and halogen element is contained at concentration not higher than 1 x 10^{20} cm^{-3}, and wherein the semiconductor device includes a p-channel thin film transistor having a mobility in a range of 200-400 cm^2/Vs. (See, for example, Figs. 2A, 2B, 4B, and 7, and related discussions on page 21, third and fourth paragraphs).

Independent claim 93 relates to a semiconductor device comprising a crystalline semiconductor island on an insulating surface, source and drain regions in said semiconductor island, a channel forming region (See, for example, reference number 109 in Fig. 3C) between said source and drain regions, a gate insulating film (See, for example, reference number 112 in Fig. 3C) adjacent to at least said channel forming region, and a gate electrode (See, for example, reference number 113 in Fig. 3C) adjacent to said channel forming region having said gate insulating film therebetween, wherein said channel forming region is formed in a monodomain region (See, for example, reference number 104 in Fig. 2B) which contains no grain boundary, wherein said crystalline semiconductor island includes at least one of hydrogen and halogen element at concentration not higher than 1 x 10^{20} cm^{-3}, and wherein the semiconductor device includes at least one n-channel thin film transistor having a mobility in a range of 500-1000 cm^2/Vs. (See, for example, Figs. 2A, 2B, 4B, and 7, and related discussions on page 21, third and fourth paragraphs).

Independent claim 99 relates to a semiconductor device comprising a p-channel thin film transistor, an n-channel thin film transistor, each of said p-channel thin film transistor and said n-channel thin film transistor comprising a crystalline semiconductor island on an insulating surface, source and drain regions in said semiconductor island, a channel forming region (See, for example, reference number 109 in Fig. 3C) between said source and drain regions, a gate insulating film (See, for example, reference number 112 in Fig. 3C) adjacent to at least said channel forming region, and a gate electrode (See, for example, reference number 113 in Fig. 3C) adjacent to said channel forming region having said gate insulating film therebetween, wherein said crystalline semiconductor island is formed in a monodomain region (See, for example, reference number 104 in Fig. 2B) which contains no grain boundary, and wherein said crystalline semiconductor island includes at least one of hydrogen and halogen element at concentration not higher than 1×10^{20} cm^{-3}. (See, for example, Figs. 2A, 2B, 4B, and 7, and related discussions on page 21, third and fourth paragraphs).

Independent claim 105 relates to a semiconductor device comprising a p-channel thin film transistor, an n-channel thin film transistor, each of said p-channel thin film transistor and said n-channel thin film transistor comprising a crystalline semiconductor island on an insulating surface, source and drain regions in said semiconductor island, a channel forming region (See, for example, reference number 109 in Fig. 3C) between said source and drain regions, a gate insulating film (See, for example, reference number 112 in Fig. 3C) adjacent to at least said channel forming region, and a gate electrode (See, for example, reference number 113 in Fig. 3C) adjacent to said channel forming region having said gate insulating film therebetween, wherein said crystalline semiconductor island includes carbon at a concentration not higher than 5×10^{18} cm^{-3}, wherein said channel forming region is formed in a monodomain region (See, for example, reference number 104 in Fig. 2B) which contains no grain boundary, and wherein said crystalline semiconductor island includes at least one of hydrogen and halogen element at concentration not higher than 1×10^{20} cm^{-3}. (See, for example, Figs. 2A, 2B, 4B, and 7, and related discussions on page 21, third and fourth paragraphs).

Independent claim 111 relates to a semiconductor device comprising an active matrix circuit portion including at least a first thin film transistor, a driving circuit portion including at least a second thin film transistor, said second thin film transistor comprising a crystalline semiconductor island on an insulating surface, source and drain regions in said semiconductor island, a channel forming region (See, for example, reference number 109 in Fig. 3C) between said source and drain regions, a gate insulating film (See, for example, reference number 112 in Fig. 3C) adjacent to at least said channel forming region, and a gate electrode (See, for example, reference number 113 in Fig. 3C) adjacent to said channel forming region having said gate insulating film therebetween, wherein said crystalline semiconductor island is formed in a monodomain region (See, for example, reference number 104 in Fig. 2B) which contains no grain boundary, and wherein said crystalline semiconductor island includes at least one of hydrogen and halogen element at concentration not higher than 1×10^{20} cm^{-3}. (See, for example, Figs. 2A, 2B, 4B, and 7, and related discussions on page 21, third and fourth paragraphs).

Independent claim 123 relates to a semiconductor device comprising a crystalline semiconductor island on an insulating surface, source and drain regions in said semiconductor island, a channel forming region (See, for example, reference number 109 in Fig. 3C) between said source and drain regions, a gate insulating film (See, for example, reference number 112 in Fig. 3C) adjacent to at least said channel forming region, and a gate electrode (See, for example, reference number 113 in Fig. 3C) adjacent to said channel forming region having said gate insulating film therebetween, wherein said crystalline semiconductor island includes carbon and nitrogen at a concentration not higher than 5×10^{18} cm^{-3}, wherein said crystalline semiconductor island is formed in a monodomain region (See, for example, reference number 104 in Fig. 2B) which contains no grain boundary, wherein said semiconductor device has a S value of 0.03-0.3, wherein said crystalline semiconductor island includes at least one of hydrogen and halogen element at concentration not higher than 1×10^{20} cm^{-3}, wherein the semiconductor device includes at least one selected from the group consisting of a p-channel thin film transistor and an n-channel thin film transistor, and wherein the p-channel thin film transistor has a mobility in a range of 200-400 cm^2/Vs while the n-channel thin film transistor has a mobility in a range of 500-1000 cm^2/Vs. (See, for example, Figs. 2A, 2B, 4B, and 7, and related discussions on page 21, third and fourth paragraphs).

Independent claim 129 relates to a semiconductor device comprising a crystalline semiconductor island on an insulating surface, source and drain regions in said semiconductor island, a channel forming region (See, for example, reference number 109 in Fig. 3C) between said source and drain regions, a gate insulating film (See, for example, reference number 112 in Fig. 3C) adjacent to at least said channel forming region, and a gate electrode (See, for example, reference number 113 in Fig. 3C) adjacent to said channel forming region having said gate insulating film therebetween, wherein said crystalline semiconductor island includes carbon and nitrogen at a concentration not higher than 5×10^{18} cm^{-3}, wherein said channel forming region is formed in a monodomain region (See, for example, reference number 104 in Fig. 2B) which contains no grain boundary, wherein said semiconductor device has a S value of 0.03-0.3, wherein said crystalline semiconductor island includes at least one of hydrogen and halogen element at concentration not higher than 1×10^{20} cm^{-3}, wherein the semiconductor device includes at least one selected from the group consisting of a p-channel thin film transistor and an n-channel thin film transistor, and wherein the p-channel thin film transistor has a mobility in a range of 200-400 cm^2/Vs while the n-channel thin film transistor has a mobility in a range of 500-1000 cm^2/Vs. (See, for example, Figs. 2A, 2B, 4B, and 7, and related discussions on page 21, third and fourth paragraphs).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The ground of rejection to be reviewed on appeal is the rejection of claims 73-116, 123-141, and 143-155 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,563,426 to Zhang et al. (hereinafter referred to as Zhang).

VII. ARGUMENTS

Appellants respectfully contend that the Examiner has failed to set forth a *prima facie* case of obviousness, since the applied Zhang reference fails to teach, disclose or suggest all limitations recited in the claimed invention. Specifically, Zhang does not teach, disclose, or suggest a channel-forming region having no grain boundary, that a channel forming region is formed in a monodomain region which contains no grain boundary, or that a crystalline semiconductor island is formed in a monodomain region which contains no grain boundary,

as recited in the claims. Accordingly, Zhang does not render the claimed invention obvious under 35 U.S.C. §103.

The Supreme Court, in *Graham v. John Deere*, set forth the basic test for patentability under 35 U.S.C. §103.[1]

> Under §103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or non-obviousness of the subject matter is determined. Such secondary considerations as commercial success, long felt but unresolved need, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter to be patented.

Moreover, in *In re Ehrreich and Avery*, the Court of Customs and Patent Appeals further clarified the basic test set forth in *Graham v. John Deere*.[2]

> We must not here consider a reference in a vacuum, but against the background of the other references of record which may disprove theories and speculations in the reference or reveal previously undiscovered or unappreciated problems. The question in a §103 case is what the references would collectively suggest to one of ordinary skill in the art. *In re Simon*, 461 F.2d 1387, 174 USPQ 114 (CCPA 1972). It is only by proceeding in this manner that we may fairly determine the scope and content of the prior art according to the mandate of *Graham v. John Deere*, 383 US 1, 17, 148 USPQ 459, 467 (1966)(Emphasis in original.)

It should be noted that three criteria must be met to establish a *prima facie* case of obviousness.[3] First, there must be some teaching, suggestion or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art.[4] Second, there must be a reasonable expectation of success.[5] Last, the prior art must teach or suggest all the claim limitations.[6]

---

[1] See *Graham v. John Deere*, 383 U.S. 1 at 18, 148 USPQ 459 at 167 (1996)

[2] See *In re Ehrreich and Avery*, 200 USPQ 504, 509-510 (CCPA 1979)

[3] See *M.P.E.P. §2143*

[4] See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

[5] See *In re Rhinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976)

[6] See *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

With respect to the present application, Appellants contend that the Examiner has failed to set forth a *prima facie* case of obviousness. In particular, Zhang fails to teach, disclose or suggest all of the limitations recited in the claimed invention. Specifically, Zhang does not teach, disclose, suggest, or inherently provide a channel-forming region having *no grain boundary*, a channel forming region formed in a monodomain region which contains *no grain boundary*, or a crystalline semiconductor island formed in a monodomain region which contains *no grain boundary*, as recited in the claims of the present application. Accordingly, Zhang does not render the claimed invention obvious under 35 U.S.C. §103.

Specifically, Zhang fails to teach, disclose, suggest, or inherently provide a thin film transistor having a channel forming region between source and drain regions, wherein the "channel forming region has no grain boundary," as recited in independent claims 73 and 80. Similarly, Zhang fails to teach, disclose, suggest, or inherently provide a channel-forming region formed in a monodomain region, wherein the "channel forming region is formed in a monodomain region which contains no grain boundary," as recited in independent claims 93, 105, and 129. Moreover, Zhang fails to teach, disclose, suggest, or inherently provide a crystalline semiconductor island formed in a monodomain region, wherein the "crystalline semiconductor island is formed in a monodomain region which contains no grain boundary," as recited in independent claims 87, 99, 111, and 123.

In the Final Office Action mailed February 17, 2005, the Examiner rejected each pending claim in a lengthy rejection spanning 36 pages. The rejection is substantially identical to the rejections made in the prior Office Actions of September 25, 2003, March 22, 2004, and October 15, 2004. In each of these Office Actions, and in the Final Office Action, the Examiner rejected all of the pending claims under 35 U.S.C. §103 in view of Zhang.

Throughout prosecution of this application, Appellants have repeatedly stressed the importance of the most distinguishing feature of the claimed invention. In particular, *the distinguishing feature of the invention resides in the formation of the active layer or the channel region within one monodomain region which contains no grain boundary.*[7]

[7] See Appellant's Response filed January 26, 2004 and Amendments filed August 18, 2004 and January 18, 2005.

In making his final rejection, the Examiner concluded, with reference to each of independent claims 73 and 80, that "Zhang discloses in figures 1a-1c, 2a-2d, and 4a-4c a gate electrode adjacent to said channel forming region having said gate insulating film therebetween, wherein said channel forming region has no grain boundary."[8] In addition, with reference to independent claims 87, 99, 111, and 123, the Examiner concluded that "Zhang discloses in figures 1a-1c, 2a-2d, and 4a-4c a gate electrode adjacent to said channel forming region having said gate insulating film therebetween, wherein said crystalline semiconductor island is formed in a monodomain region which contains no grain boundary."[9] Similarly, with respect to independent claims 93, 105, and 129, the Examiner concluded that "Zhang discloses in figures 1a-1c, 2a-2d, and 4a-4c a gate electrode adjacent to said channel forming region having said gate insulating film therebetween...wherein said channel forming region is formed in a monodomain region which contains no grain boundary."[10]

In addition, the Examiner states that Zhang shows in figure 1c wherein the channel forming region has no grain boundary and that Zhang shows in figure 1c wherein the channel forming region, under gate 7, on the islands 6, are not formed over the grain boundaries 4. Furthermore, while discounting a teaching reference, U.S. Patent No. 6,011,275 issued to Ohtani et al. (Ohtani), previously submitted by Appellants, the Examiner asserts that "irrespective of how Ohtani formed grain boundaries, at the time of the present invention and Zhang, one of ordinary skill in the art would recognize only that no grain boundary exist in the channel forming regions in the method of Zhang." However, where the prior art provides "only general guidance and is not specific as to the particular form of the invention or how to achieve it, [such a suggestion] may make an approach 'obvious to try,' but it does not make the invention obvious."[11] Nonetheless, besides making these broad, conclusory assertions, the Examiner has not clearly asserted or presented any evidence indicating that the device of Zhang has channel forming regions having no grain boundary. In addition, the Examiner has admittedly failed to understand why Zhang is incapable of forming a channel forming region having no grain boundary in view of the teaching references.

---

[8] See pages 3 and 5 of the Final Office Action dated February 17, 2005.

[9] See pages 8, 13, 17, and 19 of the Final Office Action dated February 17, 2005.

[10] See pages 10, 15, and 23 of the Final Office Action dated February 17, 2005.

[11] See *Ex parte Obukowicz*, 27 USPQ2d, 1063, 1065 (U.S. Patent and Trademark Office Board of Appeals and Interferences, 1992) and *In re O'Farrell*, 7 USPQ2d 1673, 1681 (Fed. Cir. 1988).

Throughout prosecution of this application, Appellants have repeatedly and convincingly argued that Zhang fails to teach, disclose, or suggest a channel forming region having no grain boundary.

In particular, although Zhang discloses thin film transistors arranged so that semiconductor regions 6 do not cross boundaries 4 as shown in Fig. 1(C), Zhang does not suggest or disclose the feature of the claimed invention wherein a channel forming region has no grain boundary as recited in the claims. Further, the semiconductor regions 6 of Zhang include grain boundaries because crystals inherently grow in a particular direction from island nickel regions 2. In particular, the semiconductor regions 6, which are formed in the shaded portion 3 of Zhang, include grain boundaries, since crystal grains grow radially from the island nickel region 2 and grain boundaries are generated along with the crystal growth. This direction of crystal growth was illustrated in hand-drawn directional arrows in Fig. 1(B) of Zhang, which was previously submitted with Appellants' Amendment of January 26, 2004. A copy of this drawing is submitted in the Evidence Appendix attached hereto. That is, although Zhang et al. disclose that each of semiconductor regions 6 is formed so as to avoid the grain boundaries 4, each of which is formed by collision of crystal grains grown from each of the island nickel regions 2, Zhang et al. do not disclose or suggest that each of semiconductor regions 6 is formed so as to avoid grain boundaries formed in the shaded portion 3, as noted above.

In further support of this contention, teaching references were provided to the Examiner, specifically, Ohtani and U.S. Patent No. 5,894,137 issued to Yamazaki et al. (Yamazaki). In this regard, e.g., Fig. 2A and column 4, lines 38-57 of Ohtani and, and Fig. 5A, 5B, and column 8, lines 27-51, of Yamazaki illustrate crystal growth and its relationship with grain boundary in a method such as that taught by Zhang. These references explain that crystal grains formed in a method such as Zhang's grow radially from the deposited metal, that grain boundaries are generated along with the crystal growth, and that a channel region inherently includes grain boundaries. In particular, the density of a metal element, the amount of the metal element, and the like may change when an introducing method of the metal element is changed. Furthermore, a phenomenon occurs wherein a crystal nuclei as a basis of crystal growth is formed in an amorphous silicon film by introducing the metal element and crystals grow from the nuclei. This phenomenon occurs irrespective of whether

the deposited metal is formed by a sputtering method or whether the metal element added region is formed by a method of coating a solvent containing the metal element.

In this regard, Ohtani teaches that there are various methods of introducing a metal element including, for example, "a method of coating a solvent containing the metal elements, a method using a CVD method, a method using a sputtering method or a vapor deposition method, a method conducting a plasma processing using an electrode containing the metal, and a method using a gas adsorbing method." (Col. 6, lines 24-29). The crystal grains of Zhang grow radially from the deposited metal, grain boundaries are generated along with the crystal growth as disclosed by Ohtani, and the resulting a channel region includes grain boundaries.

Accordingly, Appellants strenuously disagree with the assertions made by the Examiner that Zhang teaches a channel forming region having no grain boundary. Instead, Appellants submit that Zhang fails to teach, disclose, suggest, or inherently provide a thin film transistor having a channel forming region between source and drain regions, wherein the "channel forming region has no grain boundary," as recited in independent claims 73 and 80, a channel-forming region formed in a monodomain region, wherein the "channel forming region is formed in a monodomain region which contains no grain boundary," as recited in independent claims 93, 105, and 129, or a crystalline semiconductor island formed in a monodomain region, wherein the "crystalline semiconductor island is formed in a monodomain region which contains no grain boundary," as recited in independent claims 87, 99, 111, and 123.

In addition, although the Examiner has not explicitly stated so, Appellants believe that the Examiner is attempting to establish that the "no grain boundary" feature of the claimed invention is inherent in Zhang, as the Examiner has not been able to specifically and distinctly point out any portions of Zhang that clearly recite a channel forming region having no grain boundary. In particular, if the Examiner had been able to find each and every feature of the claims in the teachings of Zhang, Appellants would have expected the Examiner to reject the claims under 35 U.S.C. §102 rather than 35 U.S.C. §103.

In this regard, when the Examiner makes a rejection under 35 U.S.C. §103 by asserting that the prior art product seems to be identical except that the prior art is silent as to

an inherent characteristic of the claimed invention, the Examiner must provide rationale or evidence tending to show the inherency of the missing characteristic.[12] The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic.[13] "To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient."[14] "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art."[15]

In this regard, Appellants submit that the Examiner has also failed, throughout the entire prosecution of this case, to establish the inherency of the "no grain boundary" feature of the claimed invention, at least in part by failing to provide any extrinsic evidence in an attempt to establish the inherency. To the contrary, Appellants have provided arguments and evidence in the form of teaching references to establish that the "no grain boundary" feature of the claimed invention is not only not taught by Zhang, but is also not inherent in the teachings of Zhang.

---

[12] See *M.P.E.P. §2112*

[13] See *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art); In re Oelrich, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981).

[14] See *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (citations omitted).

[15] See *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original).

Accordingly, for at least the reasons outlined above, Appellants respectfully submit that U.S. Patent No. 5,563,426 to Zhang fails to teach, suggest, or disclose, either expressly or inherently, the features of the claimed invention as recited in claims 73-116, 123-141, and 143-155. Thus, Zhang cannot render obvious the claimed invention.

Respectfully submitted,
NIXON PEABODY, LLP

Date: December 12, 2005

Jeffrey L. Costellia
Registration No. 35,483

NIXON PEABODY LLP
401 9th Street, N.W., Suite 900
Washington, DC 20004
(202) 585-5000
(202) 585-8080 (Fax)

VIII. CLAIMS APPENDIX

1-72. (Canceled).

73. (Previously Presented) A thin film transistor comprising:

a crystalline semiconductor island over a substrate having an insulating surface;

source and drain regions in said semiconductor island;

a channel forming region between said source and drain regions;

a gate insulating film adjacent to at least said channel forming region;

a gate electrode adjacent to said channel forming region having said gate insulating film therebetween,

wherein said channel forming region has no grain boundary, and

wherein said semiconductor island includes a spin density not higher than 1×10^{17} cm^{-3},

wherein said crystalline semiconductor island includes at least one of hydrogen and halogen element at concentration not higher than 1×10^{20} cm^{-3}.

74. (Previously Presented) A thin film transistor according to claim 73 wherein said crystalline semiconductor island comprises a material selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Ag, Au.

75. (Previously Presented) A thin film transistor according to claim 74 wherein said material is included in said semiconductor island at a concentration not higher than 5×10^{19} cm^{-3}.

76. (Previously Presented) A thin film transistor according to claim 73 wherein said semiconductor island includes the point defect of 1×10^{16} cm^{-3} or more, and the one of hydrogen and halogen element for neutralizing the point defect at a concentration of 1×10^{15} to 1×10^{20} cm^{-3}.

77. (Previously Presented) A thin film transistor according to claim 73 wherein said semiconductor island includes the spin density not lower than 1×10^{15} cm^{-3}.

78. (Previously Presented) A thin film transistor according to claim 73 wherein said semiconductor island is a silicon island.

79. (Previously Presented) A thin film transistor according to claim 73 wherein said crystalline semiconductor island includes carbon and nitrogen at a concentration not lower than 1×10^{16} cm^{-3}, and oxygen at a concentration not lower than 1×10^{17} cm^{-3}.

80. (Previously Presented) A thin film transistor comprising:

a crystalline semiconductor island on an insulating surface;

source and drain regions in said semiconductor island;

a channel forming region between said source and drain regions;

a gate insulating film on at least said channel forming region;

a gate electrode over said channel forming region having said gate insulating film therebetween,

wherein said channel forming region has no grain boundary, and

wherein said semiconductor island includes a point defect of 1×10^{16} cm^{-3} or more, and at least one of hydrogen and halogen element at concentration not higher than 1×10^{20} cm^{-3}.

81. (Previously Presented) A thin film transistor according to claim 80 wherein said crystalline semiconductor island comprises a material selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Ag, Au.

82. (Previously Presented) A thin film transistor according to claim 80 wherein said material is included in said semiconductor island at a concentration not higher than 5×10^{19} cm^{-3}.

83. (Previously Presented) A thin film transistor according to claim 80 wherein said semiconductor island includes said one of hydrogen and halogen element for neutralizing the point defect at a concentration not lower than 1×10^{15} cm^{-3}.

84. (Previously Presented) A thin film transistor according to claim 80 wherein said semiconductor island includes a spin density of 1×10^{15} to 1×10^{17} cm^{-3}.

85. (Previously Presented) A thin film transistor according to claim 80 wherein said semiconductor island is a silicon island.

86. (Previously Presented) A thin film transistor according to claim 80 wherein said crystalline semiconductor island includes carbon and nitrogen at a concentration not lower than 1×10^{16} cm^{-3}, and oxygen at a concentration not lower than 1×10^{17} cm^{-3}.

87. (Previously Presented) A semiconductor device comprising:

a crystalline semiconductor island on an insulating surface;

source and drain regions in said semiconductor island;

a channel forming region between said source and drain regions;

a gate insulating film adjacent to at least said channel forming region;

a gate electrode adjacent to said channel forming region having said gate insulating film therebetween,

wherein said crystalline semiconductor island is formed in a monodomain region which contains no grain boundary,

wherein at least one of hydrogen and halogen element is contained at concentration not higher than 1×10^{20} cm^{-3},

wherein the semiconductor device includes a p-channel thin film transistor having a mobility in a range of 200-400 cm^2/Vs.

88. (Previously Presented) A device according to claim 87, wherein said crystalline semiconductor island comprises a material selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Ag, Au.

89. (Previously Presented) A device according to claim 88, wherein said material is included in said semiconductor island at a concentration not higher than 5×10^{19} cm^{-3}.

90. (Previously Presented) A device according to claim 87, wherein said semiconductor island is a silicon island.

91. (Previously Presented) A device according to claim 87, wherein said crystalline semiconductor island includes carbon and nitrogen at a concentration not lower than 1×10^{16} cm^{-3}, and oxygen at a concentration not lower than 1×10^{17} cm^{-3}.

92. (Previously Presented) A device according to claim 87, wherein said monodomain region has a grain size of 50 μm or more.

93. (Previously Presented) A semiconductor device comprising:

a crystalline semiconductor island on an insulating surface;

source and drain regions in said semiconductor island;

a channel forming region between said source and drain regions;

a gate insulating film adjacent to at least said channel forming region;

a gate electrode adjacent to said channel forming region having said gate insulating film therebetween,

wherein said channel forming region is formed in a monodomain region which contains no grain boundary,

wherein said crystalline semiconductor island includes at least one of hydrogen and halogen element at concentration not higher than 1×10^{20} cm^{-3},

wherein the semiconductor device includes at least one n-channel thin film transistor having a mobility in a range of 500-1000 cm^2/Vs.

94. (Previously Presented) A device according to claim 93, wherein said crystalline semiconductor island comprises a material selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Ag, Au.

95. (Previously Presented) A device according to claim 93, wherein said material is included in said semiconductor island at a concentration not higher than 5×10^{19} cm^{-3}.

96. (Previously Presented) A device according to claim 93, wherein said semiconductor island is a silicon island.

97. (Previously Presented) A device according to claim 93, wherein said crystalline semiconductor island includes carbon and nitrogen at a concentration not lower than 1×10^{16} cm^{-3}, and oxygen at a concentration not lower than 1×10^{17} cm^{-3}.

98. (Previously Presented) A device according to claim 93, wherein said monodomain region has a grain size of 50 μm or more.

99. (Previously Presented) A semiconductor device comprising:

a p-channel thin film transistor;

an n-channel thin film transistor;

each of said p-channel thin film transistor and said n-channel thin film transistor comprising:

a crystalline semiconductor island on an insulating surface;

source and drain regions in said semiconductor island;

a channel forming region between said source and drain regions;

a gate insulating film adjacent to at least said channel forming region;

a gate electrode adjacent to said channel forming region having said gate insulating film therebetween,

wherein said crystalline semiconductor island is formed in a monodomain region which contains no grain boundary,

wherein said crystalline semiconductor island includes at least one of hydrogen and halogen element at concentration not higher than 1×10^{20} cm^{-3}.

100. (Previously Presented) A device according to claim 99, wherein said crystalline semiconductor island comprises a material selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Ag, Au.

101. (Previously Presented) A device according to claim 100, wherein said material is included in said semiconductor island at a concentration not higher than 5×10^{19} cm^{-3}.

102. (Previously Presented) A device according to claim 99, wherein said semiconductor island is a silicon island.

103. (Previously Presented) A device according to claim 99, wherein said crystalline semiconductor island includes carbon and nitrogen at a concentration not lower than 1×10^{16} cm^{-3}, and oxygen at a concentration not lower than 1×10^{17} cm^{-3}.

104. (Previously Presented) A device according to claim 99, wherein said monodomain region has a grain size of 50 μm or more.

105. (Previously Presented) A semiconductor device comprising:

a p-channel thin film transistor;

an n-channel thin film transistor;

each of said p-channel thin film transistor and said n-channel thin film transistor comprising:

a crystalline semiconductor island on an insulating surface;

source and drain regions in said semiconductor island;

a channel forming region between said source and drain regions;

a gate insulating film adjacent to at least said channel forming region;

a gate electrode adjacent to said channel forming region having said gate insulating film therebetween,

wherein said crystalline semiconductor island includes carbon at a concentration not higher than 5×10^{18} cm^{-3},

wherein said channel forming region is formed in a monodomain region which contains no grain boundary,

wherein said crystalline semiconductor island includes at least one of hydrogen and halogen element at concentration not higher than 1×10^{20} cm^{-3} .

106. (Previously Presented) A device according to claim 105, wherein said crystalline semiconductor island comprises a material selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Ag, Au.

107. (Previously Presented) A device according to claim 106, wherein said material is included in said semiconductor island at a concentration not higher than 5×10^{19} cm^{-3}.

108. (Previously Presented) A device according to claim 105, wherein said semiconductor island is a silicon island.

109. (Previously Presented) A device according to claim 105, wherein said crystalline semiconductor island includes carbon and nitrogen at a concentration not lower than 1×10^{16} cm^{-3}, and oxygen at a concentration not lower than 1×10^{17} cm^{-3}.

110. (Previously Presented) A device according to claim 105, wherein said monodomain region has a grain size of 50 μm or more.

111. (Previously Presented) A semiconductor device comprising:

an active matrix circuit portion including at least a first thin film transistor;

a driving circuit portion including at least a second thin film transistor;

said second thin film transistor comprising:

a crystalline semiconductor island on an insulating surface;

source and drain regions in said semiconductor island;

a channel forming region between said source and drain regions;

a gate insulating film adjacent to at least said channel forming region;

a gate electrode adjacent to said channel forming region having said gate insulating film therebetween,

wherein said crystalline semiconductor island is formed in a monodomain region which contains no grain boundary,

wherein said crystalline semiconductor island includes at least one of hydrogen and halogen element at concentration not higher than 1×10^{20} cm^{-3}.

112. (Previously Presented) A device according to claim 111, wherein said crystalline semiconductor island comprises a material selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Ag, Au.

113. (Previously Presented) A device according to claim 112, wherein said material is included in said semiconductor island at a concentration not higher than 5×10^{19} cm^{-3}.

114. (Previously Presented) A device according to claim 111, wherein said semiconductor island is a silicon island.

115. (Previously Presented) A device according to claim 111, wherein said crystalline semiconductor island includes carbon and nitrogen at a concentration not lower than 1×10^{16} cm^{-3}, and oxygen at a concentration not lower than 1×10^{17} cm^{-3}.

116. (Previously Presented) A device according to claim 111, wherein said monodomain region has a grain size of 50 μm or more.

117-122. (Canceled).

123. (Previously Presented) A semiconductor device comprising:

a crystalline semiconductor island on an insulating surface;

source and drain regions in said semiconductor island;

a channel forming region between said source and drain regions;

a gate insulating film adjacent to at least said channel forming region;

a gate electrode adjacent to said channel forming region having said gate insulating film therebetween,

wherein said crystalline semiconductor island includes carbon and nitrogen at a concentration not higher than 5×10^{18} cm^{-3},

wherein said crystalline semiconductor island is formed in a monodomain region which contains no grain boundary,

wherein said semiconductor device has a S value of 0.03-0.3,

wherein said crystalline semiconductor island includes at least one of hydrogen and halogen element at concentration not higher than 1×10^{20} cm^{-3},

wherein the semiconductor device includes at least one selected from the group consisting of a p-channel thin film transistor and an n-channel thin film transistor,

wherein the p-channel thin film transistor has a mobility in a range of 200-400 cm^2/Vs while the n-channel thin film transistor has a mobility in a range of 500-1000 cm^2/Vs.

124. (Previously Presented) A device according to claim 123, wherein said crystalline semiconductor island comprises a material selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Ag, Au.

125. (Previously Presented) A device according to claim 124, wherein said material is included in said semiconductor island at a concentration not higher than 5×10^{19} cm^{-3}.

126. (Previously Presented) A device according to claim 123, wherein said semiconductor island is a silicon island.

127. (Previously Presented) A device according to claim 123, wherein said crystalline semiconductor island includes carbon and nitrogen at a concentration not lower than 1×10^{16} cm^{-3}, and oxygen at a concentration not lower than 1×10^{17} cm^{-3}.

128. (Previously Presented) A device according to claim 123, wherein said monodomain region has a grain size of 50 μm or more.

129. (Previously Presented) A semiconductor device comprising:

a crystalline semiconductor island on an insulating surface;

source and drain regions in said semiconductor island;

a channel forming region between said source and drain regions;

a gate insulating film adjacent to at least said channel forming region;

a gate electrode adjacent to said channel forming region having said gate insulating film therebetween,

wherein said crystalline semiconductor island includes carbon and nitrogen at a concentration not higher than 5×10^{18} cm^{-3},

wherein said channel forming region is formed in a monodomain region which contains no grain boundary,

wherein said semiconductor device has a S value of 0.03-0.3,

wherein said crystalline semiconductor island includes at least one of hydrogen and halogen element at concentration not higher than 1×10^{20} cm^{-3},

wherein the semiconductor device includes at least one selected from the group consisting of a p-channel thin film transistor and an n-channel thin film transistor,

wherein the p-channel thin film transistor has a mobility in a range of 200-400 cm^2/Vs while the n-channel thin film transistor has a mobility in a range of 500-1000 cm^2/Vs.

130. (Previously Presented) A device according to claim 129, wherein said crystalline semiconductor island comprises a material selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Ag, Au.

131. (Previously Presented) A device according to claim 130, wherein said material is included in said semiconductor island at a concentration not higher than 5×10^{19} cm^{-3}.

132. (Previously Presented) A device according to claim 129, wherein said semiconductor island is a silicon island.

133. (Previously Presented) A device according to claim 129, wherein said crystalline semiconductor island includes carbon and nitrogen at a concentration not lower than 1×10^{16} cm^{-3}, and oxygen at a concentration not lower than 1×10^{17} cm^{-3}.

134. (Previously Presented) A device according to claim 129, wherein said monodomain region has a grain size of 50 μm or more.

135. (Previously Presented) A thin film transistor according to claim 73, wherein each of the concentrations of carbon, nitrogen and oxygen is measured by secondary ion mass spectroscopy (SIMS).

136. (Previously Presented) A thin film transistor according to claim 80, wherein each of the concentrations of carbon, nitrogen and oxygen is measured by secondary ion mass spectroscopy (SIMS).

137. (Previously Presented) A device according to claim 87, wherein each of the concentrations of carbon, nitrogen and oxygen is measured by secondary ion mass spectroscopy (SIMS).

138. (Previously Presented) A device according to claim 93, wherein each of the concentrations of carbon, nitrogen and oxygen is measured by secondary ion mass spectroscopy (SIMS).

139. (Previously Presented) A device according to claim 99, wherein each of the concentrations of carbon, nitrogen and oxygen is measured by secondary ion mass spectroscopy (SIMS).

140. (Previously Presented) A device according to claim 105, wherein each of the concentrations of carbon, nitrogen and oxygen is measured by secondary ion mass spectroscopy (SIMS).

141. (Previously Presented) A device according to claim 111, wherein each of the concentrations of carbon, nitrogen and oxygen is measured by secondary ion mass spectroscopy (SIMS).

142. (Canceled).

143. (Previously Presented) A device according to claim 123, wherein each of the concentrations of carbon, nitrogen and oxygen is measured by secondary ion mass spectroscopy (SIMS).

144. (Previously Presented) A device according to claim 129, wherein each of the concentrations of carbon, nitrogen and oxygen is measured by secondary ion mass spectroscopy (SIMS).

145. (Previously Presented) The thin film transistor according to claim 73 wherein said crystalline semiconductor island includes carbon and nitrogen at a concentration not higher than 5×10^{18} cm^{-3}, and oxygen at a concentration not higher than 5×10^{19} cm^{-3}.

146. (Previously Presented) The thin film transistor according to claim 73 wherein the thin film transistor is one of a p-channel thin film transistor having a mobility in a range

of 200-400 cm^2/Vs and an n-channel thin film transistor having a mobility in a range of 500-1000 cm^2/Vs.

147. (Previously Presented) The thin film transistor according to claim 80 wherein said crystalline semiconductor island includes carbon and nitrogen at a concentration not higher than 5×10^{18} cm^{-3}, and oxygen at a concentration not higher than 5×10^{19} cm^{-3}.

148. (Previously Presented) The thin film transistor according to claim 80 wherein the thin film transistor is one of a p-channel thin film transistor having a mobility in a range of 200-400 cm^2/Vs and an n-channel thin film transistor having a mobility in a range of 500-1000 cm^2/Vs.

149. (Previously Presented) The semiconductor device according to claim 87 wherein said crystalline semiconductor island includes carbon and nitrogen at a concentration not higher than 5×10^{18} cm^{-3}, and oxygen at a concentration not higher than 5×10^{19} cm^{-3}.

150. (Previously Presented) The semiconductor device according to claim 93 wherein said crystalline semiconductor island includes carbon and nitrogen at a concentration not higher than 5×10^{18} cm^{-3}, and oxygen at a concentration not higher than 5×10^{19} cm^{-3}.

151. (Previously Presented) The semiconductor device according to claim 99 wherein said crystalline semiconductor island includes carbon and nitrogen at a concentration not higher than 5×10^{18} cm^{-3}, and oxygen at a concentration not higher than 5×10^{19} cm^{-3}.

152. (Previously Presented) The semiconductor device according to claim 99 wherein the p-channel thin film transistor has a mobility in a range of 200-400 cm^2/Vs and the n-channel thin film transistor has a mobility in a range of 500-1000 cm^2/Vs.

153. (Previously Presented) The semiconductor device according to claim 105 wherein the p-channel thin film transistor has a mobility in a range of 200-400 cm^2/Vs and the n-channel thin film transistor has a mobility in a range of 500-1000 cm^2/Vs.

154. (Previously Presented) The semiconductor device according to claim 111 wherein said crystalline semiconductor island includes carbon and nitrogen at a concentration not higher than 5×10^{18} cm^{-3}.

155. (Previously Presented) The semiconductor device according to claim 111 wherein the second thin film transistor is one of a p-channel thin film transistor having a mobility in a range of 200-400 cm^2/Vs and an n-channel thin film transistor having a mobility in a range of 500-1000 cm^2/Vs.

IX. EVIDENCE APPENDIX

Figure 1(B) of Zhang with hand-drawn illustrations of the direction of crystal growth, previously submitted with Appellants' Amendment of January 26, 2004.

X. RELATED PROCEEDINGS APPENDIX

There are no related proceedings to this Appeal.